HARRIS SEMICONDUCTOR

# CA3140

## BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

April 1994

### Features

- MOSFET Input Stage
  - Very High Input Impedance ($Z_{IN}$) -1.5TΩ (Typ.)
  - Very Low Input Current ($I_I$) -10pA (Typ.) at ±15V
  - Wide Common Mode Input Voltage Range (VICR) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

### Applications

- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (µseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

### Description

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 CMOS operational amplifiers and the versatility of the 741 series of industry standard operational amplifiers.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The CA3140 Series has the same 8-lead pinout used for the “741” and other industry standard op amps. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

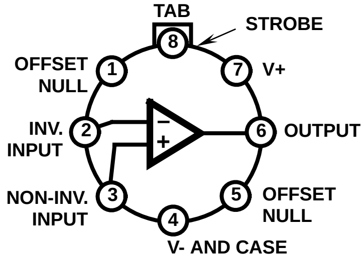
### Ordering Information

| PART NUMBER | TEMP. RANGE | PACKAGE |
|---|---|---|
| CA3140AE | $-55^oC$ to $+125^oC$ | 8 Lead Plastic DIP |
| CA3140AM | $-55^oC$ to $+125^oC$ | 8 Lead SOIC |
| CA3140AS | $-55^oC$ to $+125^oC$ | 8 Pin Can, Lead Formed |
| CA3140AT | $-55^oC$ to $+125^oC$ | 8 Pin Can |
| CA3140BT | $-55^oC$ to $+125^oC$ | 8 Pin Can |
| CA3140E | $-55^oC$ to $+125^oC$ | 8 Lead Plastic DIP |
| CA3140M | $-55^oC$ to $+125^oC$ | 8 Lead SOIC |
| CA3140M96 | $-55^oC$ to $+125^oC$ | 8 Lead SOIC* |
| CA3140T | $-55^oC$ to $+125^oC$ | 8 Pin Can |

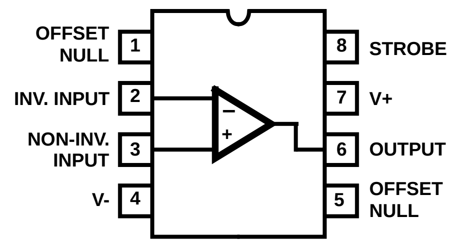
* Denotes Tape and Reel

### Pinouts

CA3140 (TO-5 STYLE CAN)
TOP VIEW




CA3140 (PDIP, SOIC)
TOP VIEW






File Number 957.2

## Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals). . . . . . . . . . 36V
Differential Mode Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . 8V
DC Input Voltage . . . . . . . . . . . . . . . . . . . . . .(V+ +8V) To (V- -0.5V)
Input Terminal Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1mA
Output Short Circuit Duration* . . . . . . . . . . . . . . . . . . . . . . . Indefinite
Junction Temperature. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . . . . . . . . . . . +150°C
Lead Temperature (Soldering 10 Sec.). . . . . . . . . . . . . . . . . . +300°C

* Short circuit may be applied to ground or to either supply.

## Operating Conditions

OperatingTemperature Range (All Types). . . . . . . . -55°C to +125°C
Storage Temperature Range (All Types). . . . . . . . . -65°C to +150°C

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications

V+ = +15V, V- = -15V, $T_A$ = +25°C

| PARAMETERS | SYMBOL | TEST CONDITIONS | | CA3140A | CA3140 | UNITS |
|---|---|---|---|---|---|---|
| Input Offset Voltage Adjustment Resistor | | Typical Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. $V_{IO}$ | | 18 | 4.7 | kΩ |
| Input Resistance | $R_I$ | | | 1.5 | 1.5 | TΩ |
| Input Capacitance | $C_I$ | | | 4 | 4 | pF |
| Output Resistance | $R_O$ | | | 60 | 60 | Ω |
| Equivalent Wideband Input Noise Voltage (See Figure 35) | $e_N$ | BW = 140kHz, $R_S$ = 1 MΩ | | 48 | 48 | µV |
| Equivalent Input Noise Voltage (See Figure 7) | $e_N$ | f = 1kHz | $R_S$ = 100Ω | 40 | 40 | nV/$\sqrt{Hz}$ |
| | | f = 10 kHz | | 12 | 12 | nV/$\sqrt{Hz}$ |
| Short Circuit Current to Opposite Supply | | | | | | |
| Source | $I_{OM}$+ | | | 40 | 40 | mA |
| Sink | $I_{OM}$- | | | 18 | 18 | mA |
| Gain-Bandwidth Product, (See Figures 2 & 15) | $f_T$ | | | 4.5 | 4.5 | MHz |
| Slew Rate, (See Figure 3) | SR | | | 9 | 9 | V/µs |
| Sink Current From Terminal 8 To Terminal 4 to Swing Output Low | | | | 220 | 220 | µA |
| Transient Response: | | $R_L$ = 2kΩ, $C_L$ = 100pF | | | | |
| Rise Time | $t_R$ | | | 0.08 | 0.08 | µs |
| Overshoot (See Figure 34) | OS | | | 10 | 10 | % |
| Settling Time at 10 $V_{P-P}$, (See Figure 14) | $t_S$ | $R_L$ = 2kΩ, $C_L$ = 100pF, Voltage Follower | | | | |
| 1mV | | | | 4.5 | 4.5 | µs |
| 10mV | | | | 1.4 | 1.4 | µs |

**Electrical Specifications** For Equipment Design. At V+ = 15V, V- = 15V, $T_A$ = +25$^oC$, Unless Otherwise Specified

| PARAMETERS | SYMBOL | LIMITS CA3140A MIN | TYP | MAX | CA3140 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $\lvert V_{IO} \rvert$ | - | 2 | 5 | - | 5 | 15 | mV |
| Input Offset Current | $\lvert I_{IO} \rvert$ | - | 0.5 | 20 | - | 0.5 | 30 | pA |
| Input Current | $I_I$ | - | 10 | 40 | - | 10 | 50 | pA |
| Large Signal Voltage Gain (Note 1) (See Figures 1, 15) | $A_{OL}$ | 20 | l00 | - | 20 | 100 | - | kV/V |
| | | 86 | 100 | - | 86 | 100 | - | dB |
| Common Mode Rejection Ratio (See Figure 6) | CMRR | - | 32 | 320 | - | 32 | 320 | µV/V |
| | | 70 | 90 | - | 70 | 90 | - | dB |
| Common Mode Input Voltage Range (See Figure 17) | $V_{ICR}$ | -15 | -15.5 to +12.5 | 12 | -15 | -15.5 to +12.5 | 11 | V |
| Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 8) | PSRR | - | 100 | 150 | - | 100 | 150 | µV/V |
| | | 76 | 80 | - | 76 | 80 | - | dB |
| Max. Output Voltage (Note 2) (See Figures 10, 17) | $V_{OM}+$ | +12 | 13 | - | +12 | 13 | - | V |
| | $V_{OM}-$ | -14 | -14.4 | - | -14 | -14.4 | - | V |
| Supply Current (See Figure 4) | I+ | - | 4 | 6 | - | 4 | 6 | mA |
| Device Dissipation | $P_D$ | - | 120 | 180 | - | 120 | 180 | mW |
| Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$ | | - | 6 | - | - | 8 | - | µV/$^o$C |

NOTES:

1. At $V_O$ = 26$V_{p-p}$, +12V, 14V and $R_L$ = 2kΩ.
2. At $R_L$ = 2kΩ.

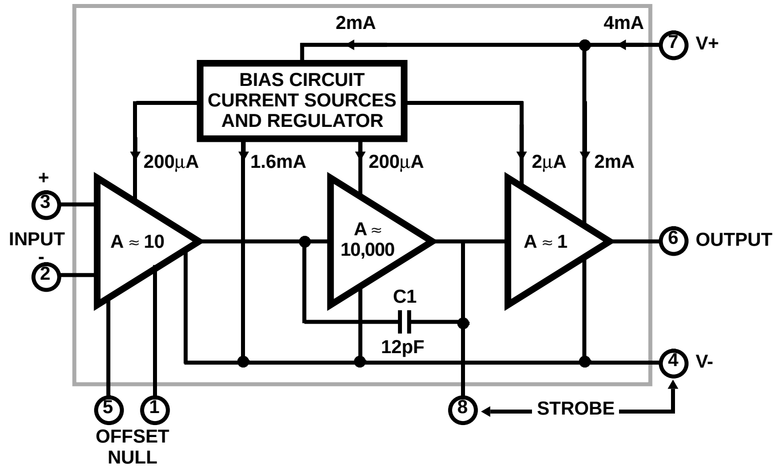
**Electrical Specifications** For Design Guidance. At V+ = 5 V, V- = 0V, $T_A$ = +25$^oC$

| PARAMETERS | SYMBOL | CA3140A | CA3140 | UNITS |
|---|---|---|---|---|
| Input Offset Voltage | $\lvert V_{IO} \rvert$ | 2 | 5 | mV |
| Input Offset Current | $\lvert I_{IO} \rvert$ | 0.1 | 0.1 | pA |
| Input Current | $I_I$ | 2 | 2 | pA |
| Input Resistance | $R_I$ | 1 | 1 | TΩ |
| Large Signal Voltage Gain (See Figures 1, 15) | $A_{OL}$ | 100 | 100 | kV/V |
| | | 100 | 100 | dB |

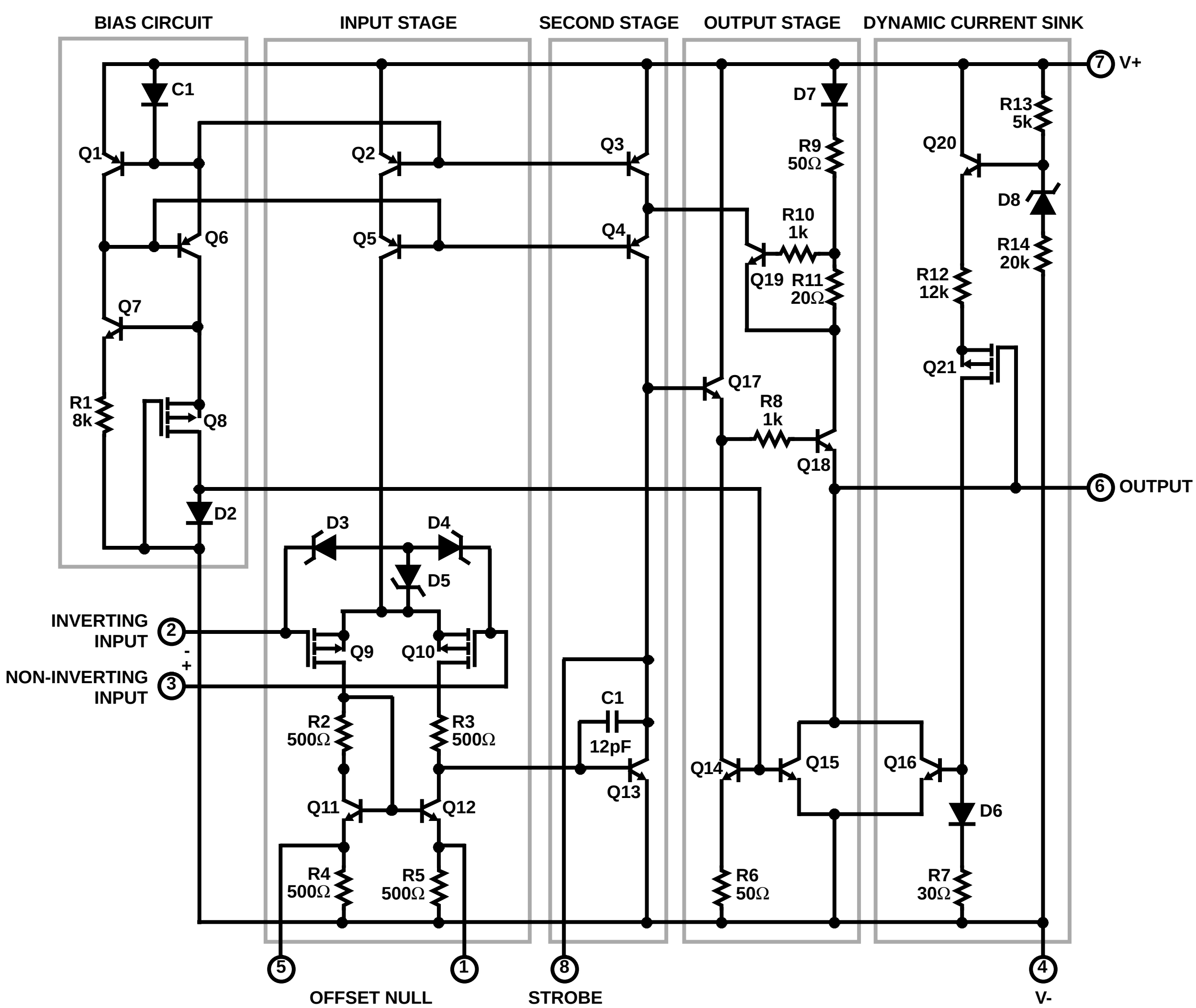
**Electrical Specifications** For Design Guidance. At V+ = 5 V, V- = 0V, $T_A$ = +25$^o$C **(Continued)**

| PARAMETERS | SYMBOL | CA3140A | CA3140 | UNITS |
|---|---|---|---|---|
| Common Mode Rejection Ratio, | CMRR | 32 | 32 | μV/V |
| | | 90 | 90 | dB |
| Common Mode Input Voltage Range (See Figure 17) | $V_{ICR}$ | -0.5 | -0.5 | V |
| | | 2.6 | 2.6 | V |
| Power Supply Rejection Ratio | PSRR $\Delta V_{I0}/\Delta V_S$ | 100 | 100 | μV/V |
| | | 80 | 80 | dB |
| Maximum Output Voltage (See Figures 10, 17) | $V_{OM}+$ | 3 | 3 | V |
| | $V_{OM}-$ | 0.13 | 0.13 | V |
| Maximum Output Current: | | | | |
| Source | IOM+ | 10 | 10 | mA |
| Sink | $I_{OM-}$ | 1 | 1 | mA |
| Slew Rate (See Figure 3) | SR | 7 | 7 | V/μs |
| Gain-Bandwidth Product (See Figure 2) | $f_T$ | 3.7 | 3.7 | MHz |
| Supply Current (See Figure 4) | I+ | 1.6 | 1.6 | mA |
| Device Dissipation | $P_D$ | 8 | 8 | mW |
| Sink Current from Term. 8 to Term. 4 to Swing Output Low | | 200 | 200 | μA |

## Block Diagram




## Schematic Diagram




ALL RESISTANCE VALUES ARE IN Ω

## Circuit Description

As shown in the block diagram, the input terminals may be operated down to 0.5V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant current flow circuits in the first and second stages. The CA3140 includes an on chip phase compensating capacitor that is sufficient for the unity gain voltage follower configuration.

**Input Stages**

The schematic diagram consists of a differential input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror pair transistors also function as a differential-to-single-ended converter to provide base current drive to the second stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode connected bipolar transistors Q2, Q5 are the constant current source for the input stage. The base biasing circuit for the constant current source is described subsequently. The small diodes D3, D4, D5 provide gate oxide protection against high voltage transients, e.g., static electricity.

**Second Stage**

Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

**Output Stage**

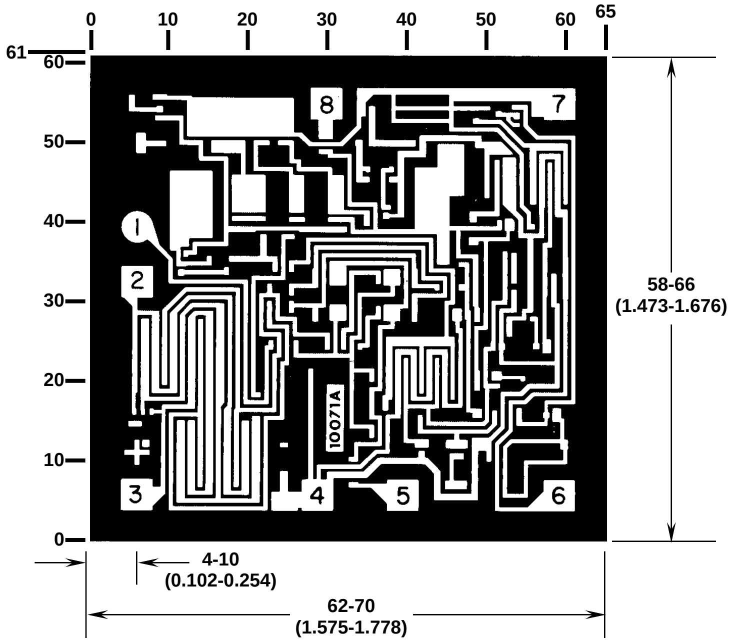
The CA3140 Series circuits employ a broad band output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base currents are “mirrored” to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V- bus, transistor Q16 is the current sinking element. Transistor Q16 is mirror connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current flow through R13, zener D8, and R14. The dynamic current sink is controlled by voltage level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential midpoint between the V+ and V- supply rails. When output current sinking mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V- bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base current drive from Q17, thereby limiting current flow in Q18 to the short circuited load terminal.

**Bias Circuit**

Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant current flow through D1, Q6, Q8 and D2. D1 is a diode connected transistor mirror connected in parallel with the base emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base currents in Q2, Q3 are also determined by constant current flow D1. Furthermore, current in diode connected transistor Q2 establishes the currents in transistors Q14 and Q15.

## Metallization Mask Layout




Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are $57^o$ instead of $90^o$ with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

## Typical Performance Curves

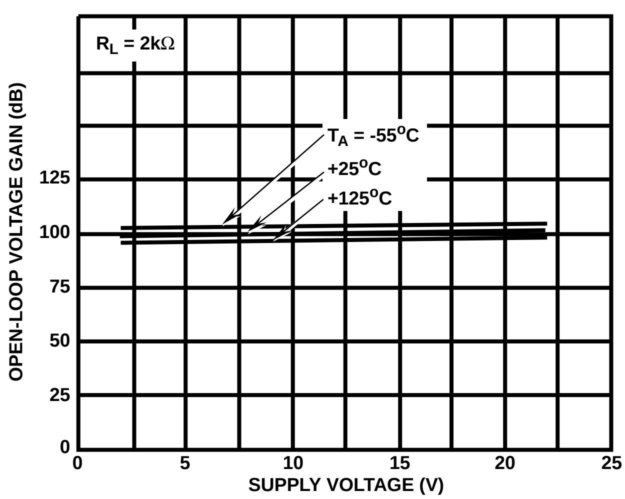



FIGURE 1. OPEN LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

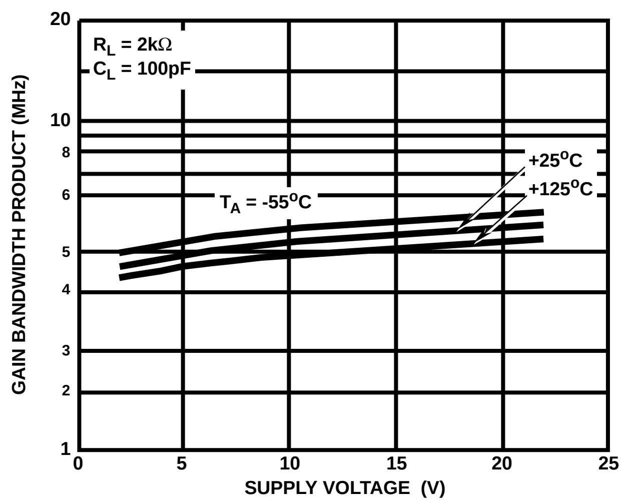



FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

## *Typical Performance Curves* (Continued)

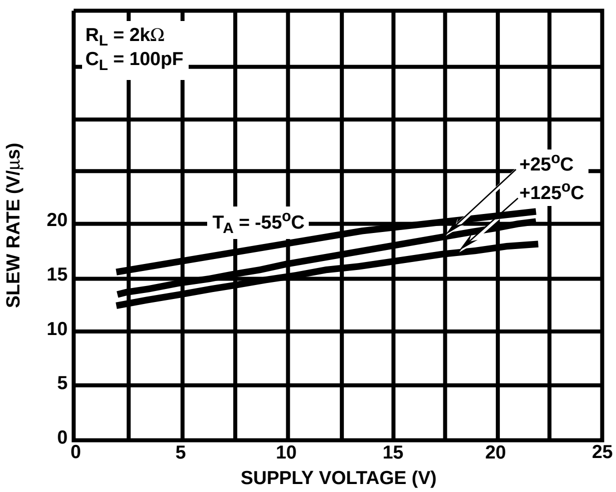



FIGURE 3. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

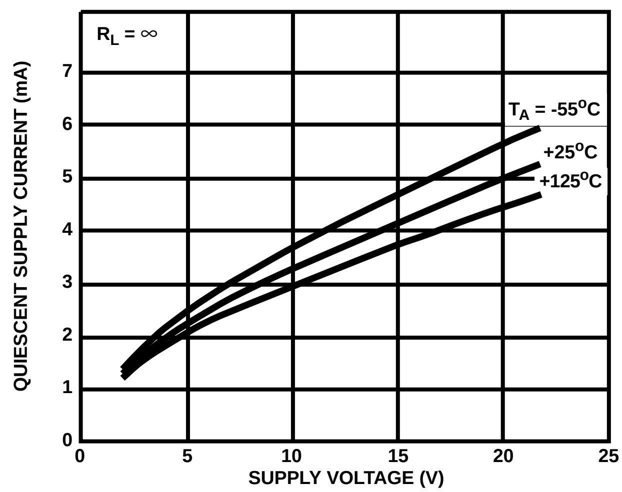



FIGURE 4. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

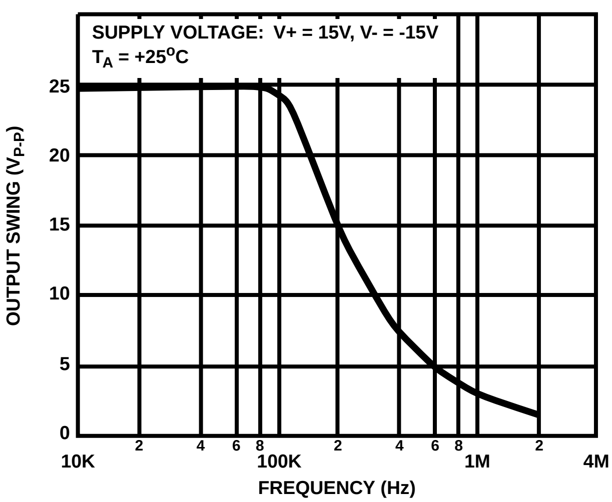



FIGURE 5. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

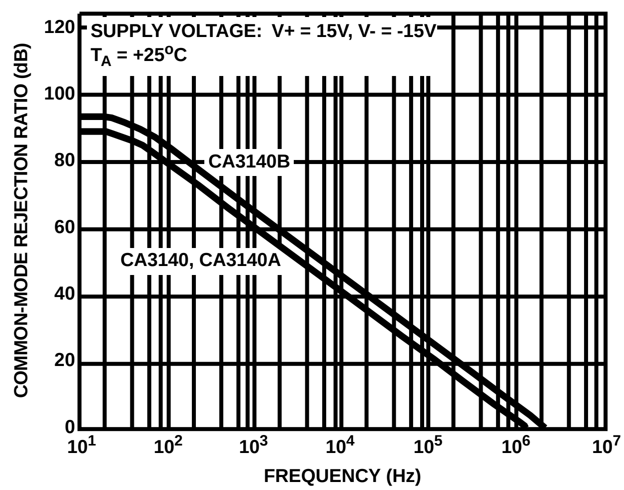



FIGURE 6. COMMON MODE REJECTION RATIO vs FREQUENCY

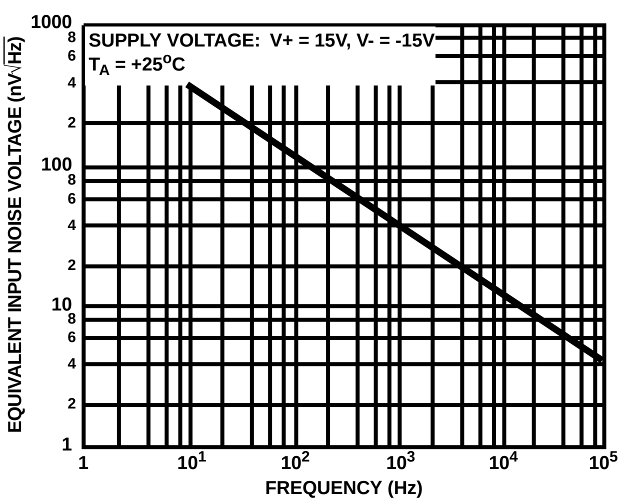



FIGURE 7. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

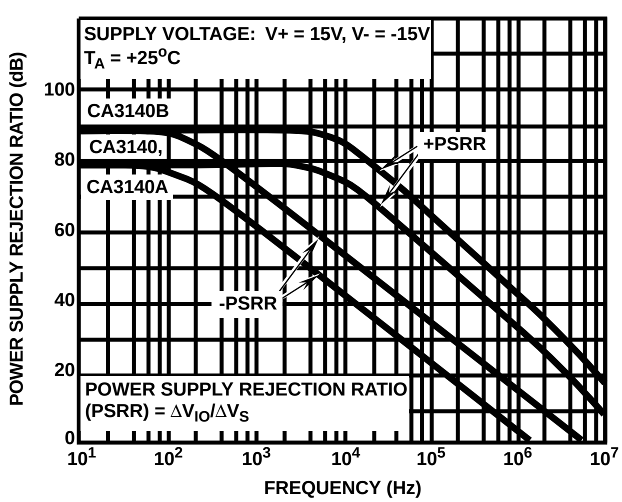



FIGURE 8. POWER SUPPLY REJECTION RATIO vs FREQUENCY

## Applications Considerations

Wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics is achieved in the CA3140 by the use of an unique design based upon the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V.

The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

### Output Circuit Considerations

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to terminal 8 as shown in Figure 9. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

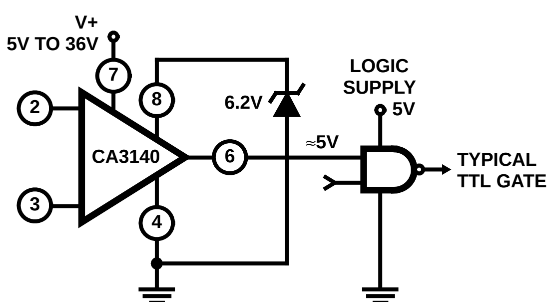



**FIGURE 9. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT CA3140 OUTPUT SWING TO TTL LEVELS**

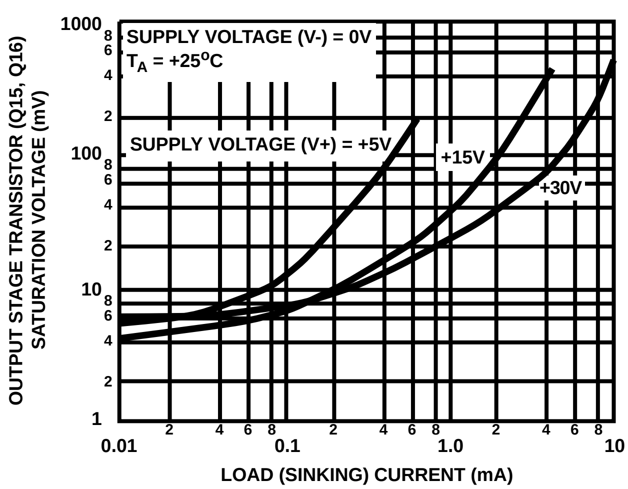



**FIGURE 10. VOLTAGE ACROSS OUTPUT TRANSISTORS Q15 AND Q16 vs LOAD CURRENT**

Figure 10 shows output current sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 13 shows some typical configurations. Note that a series resistor, $R_L$, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

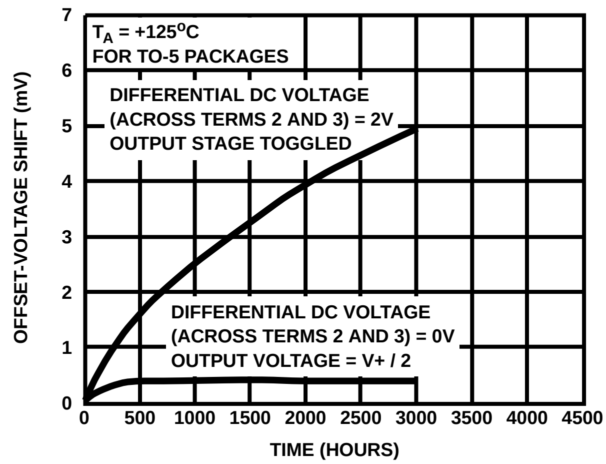



**FIGURE 11. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE**

### Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 12(A). This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Figure 12(B), to optimize its utilization range are given in the table "Electrical Specifications" shown in this bulletin.

An alternate system is shown in Figure 12(C). This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

### Low Voltage Operation

Operation at total supply voltages as low as 4V is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the

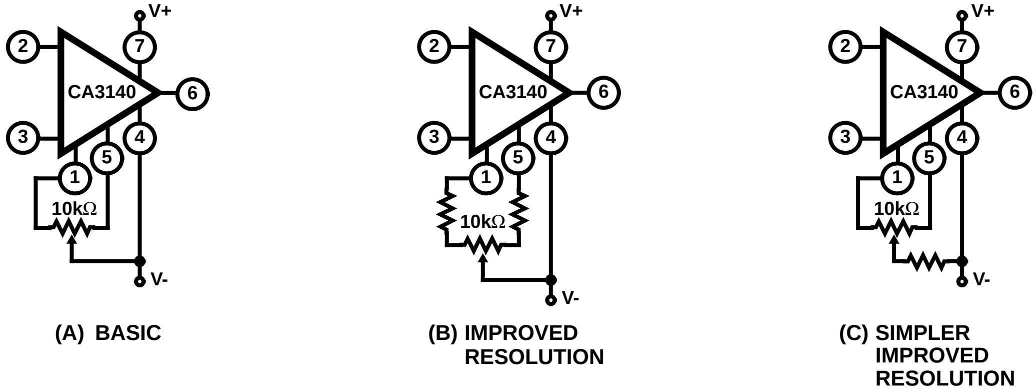



FIGURE 12. THREE OFFSET VOLTAGE NULLING METHODS

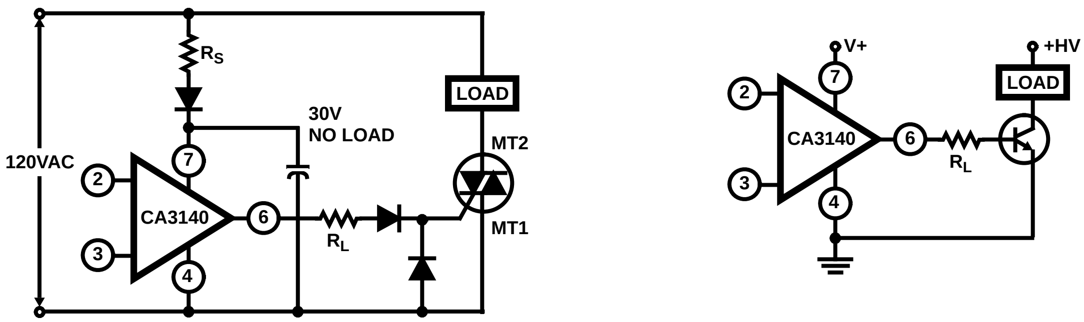



FIGURE 13. METHODS OF UTILIZING THE $V_{CE}$(SAT) SINKING CURRENT CAPABILITY OF THE CA3140 SERIES

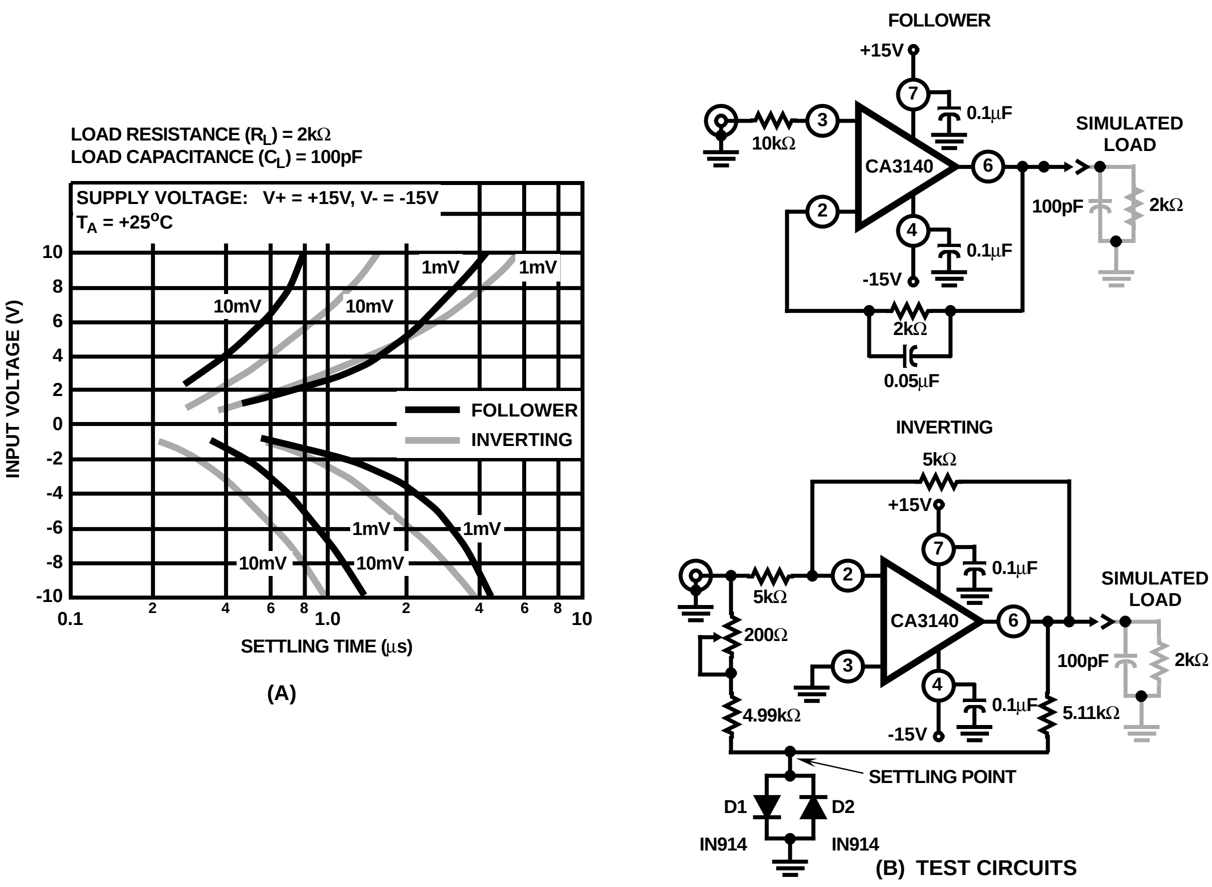



FIGURE 14. INPUT VOLTAGE vs SETTLING TIME

voltage at terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 17 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

**Bandwidth and Slew Rate**

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 14 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers. The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Figure 15.

**Input Circuit Considerations**

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and directly driving the internal constant current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

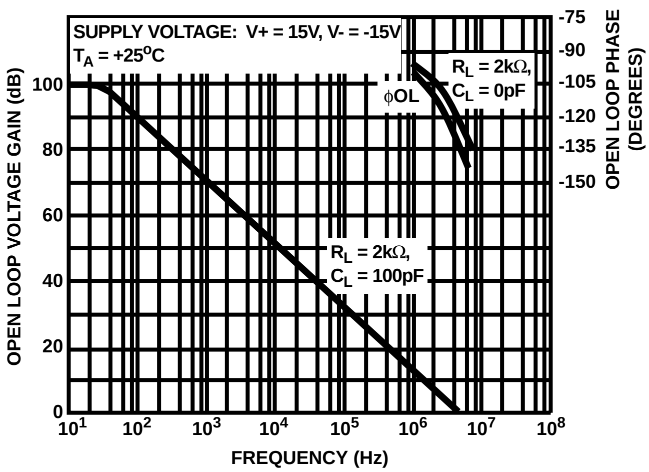



FIGURE 15. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

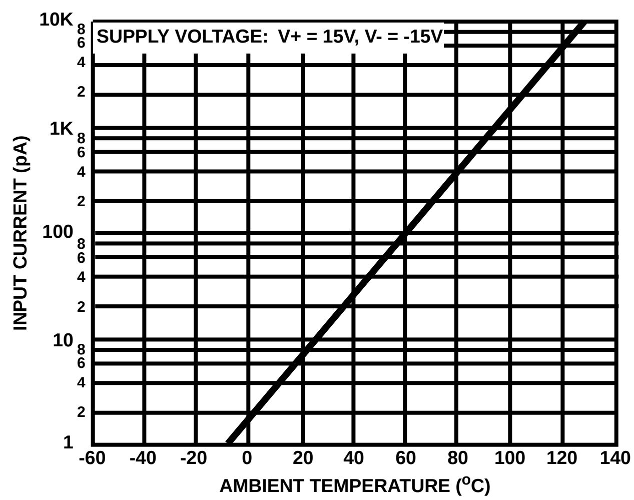



FIGURE 16. INPUT CURRENT vs AMBIENT TEMPERATURE

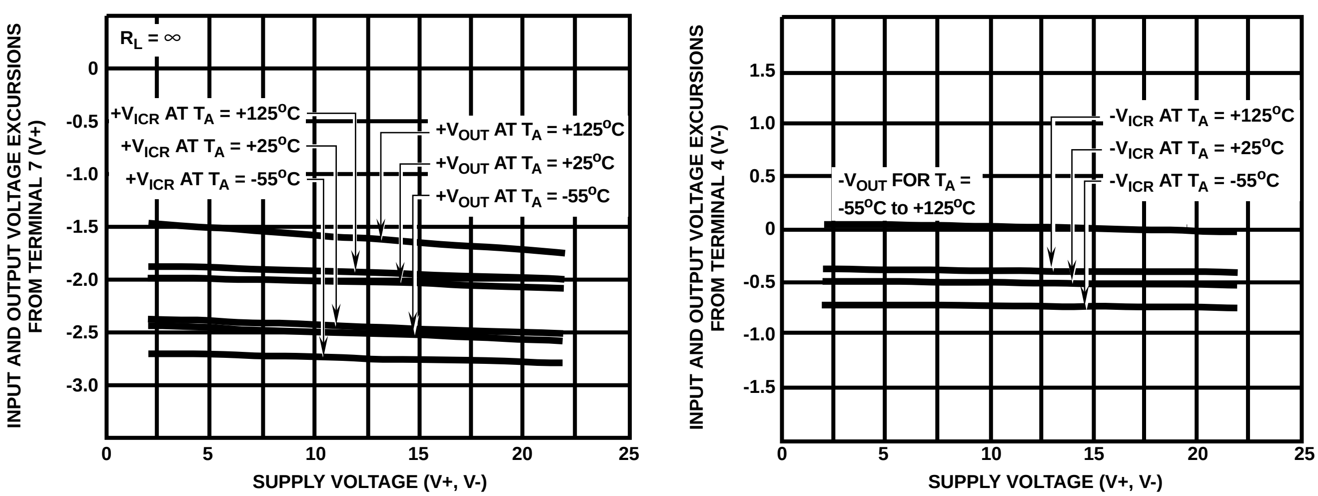



FIGURE 17. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE AND TEMPERATURE

The typical input current is in the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Figure 16 shows typical input terminal current versus ambient temperature for the CA3140.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Figure 11 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of +125$^o$C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at +85$^o$C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

**Super Sweep Function Generator**

A function generator having a wide tuning range is shown in Figure 18. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting readout amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high speed hysteresis switch. Output from the switch is returned directly back to the input of the CA3080A current source, thereby, completing the positive feedback loop

The triangular output level is determined by the four 1N914 level limiting diodes of the second CA3080 and the resistor divider network connected to terminal No. 2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High frequency ramp linearity is adjusted by the single 7-to-6pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA3080A is characterized for maximum output linearity in the current generator function.

**Meter Driver and Buffer Amplifier**

Figure 19 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60mV change in the applied voltage, $V_{ABC}$ (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360mV change in $V_{ABC}$.

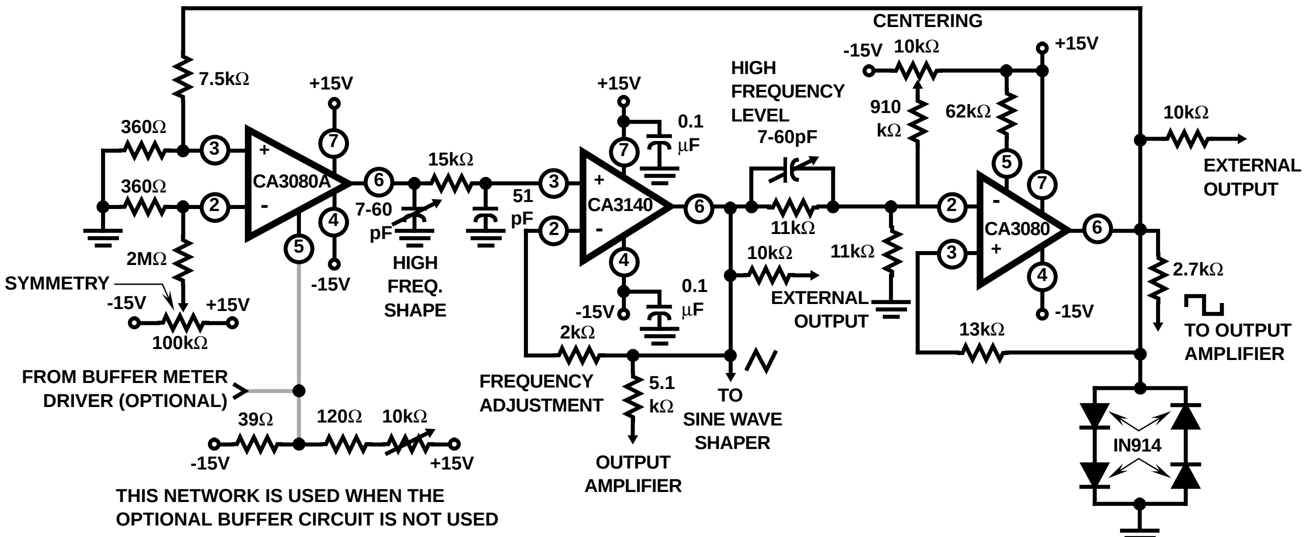
Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A $V_{ABC}$ terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

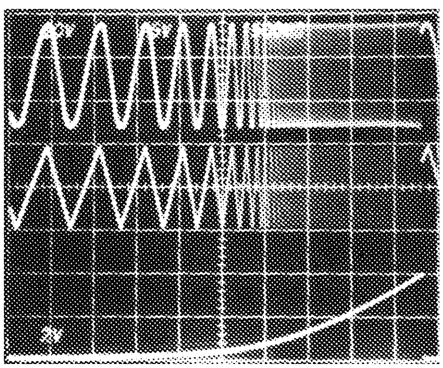
To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necessary. Two adjustments are used for the meter. The meter sensitivity control sets the meter scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects $^1/_6$ of full scale for each decade change in frequency.

**Sine Wave Shaper**

The circuit shown in Figure 20 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero crossing slope is established by the 10kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1kΩ resistor and 10kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes $D_1$ through $D_4$. Positive feedback via $D_5$ and $D_6$ establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.




(A) CIRCUIT

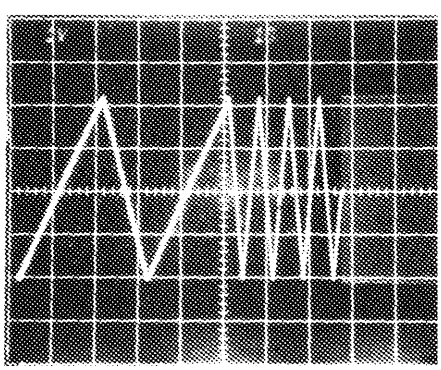


**(B1) FUNCTION GENERATOR SWEEPING**

Top Trace: Output at junction of 2.7Ω and 51Ω resistors 5V/Div and 500ms/Div

Center Trace: External output of triangular function generator 2V/Div and 500ms/Div

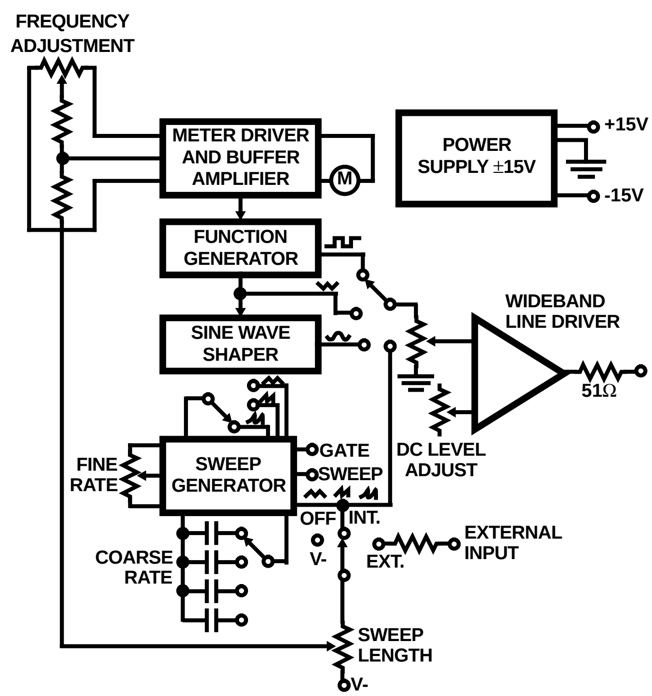
Bottom Trace: Output of “Log” generator; 10V/Div and 500ms/Div



**(B2) FUNCTION GENERATOR WITH FIXED FREQUENCIES**

1V/Div and 1sec/Div

Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100pA level.




**(C) INTERCONNECTIONS**

**FIGURE 18. FUNCTION GENERATOR**

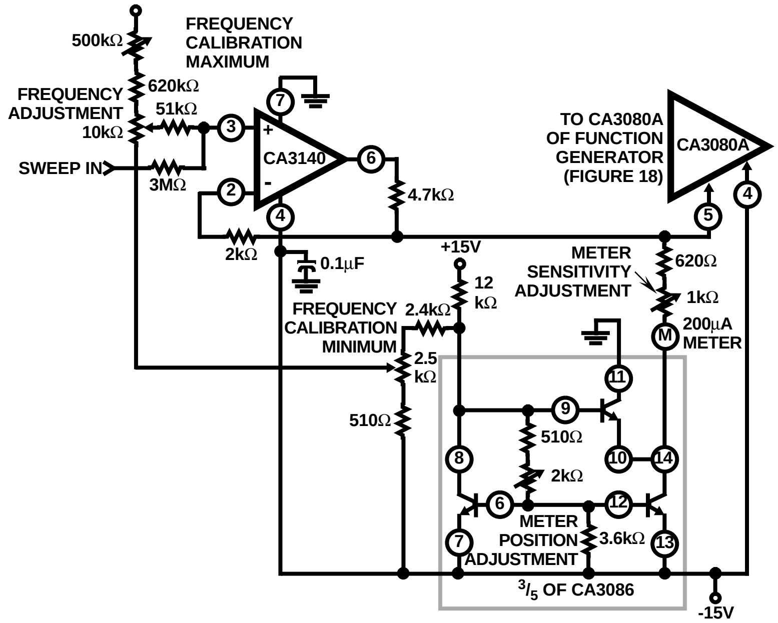



FIGURE 19. METER DRIVER AND BUFFER AMPLIFIER

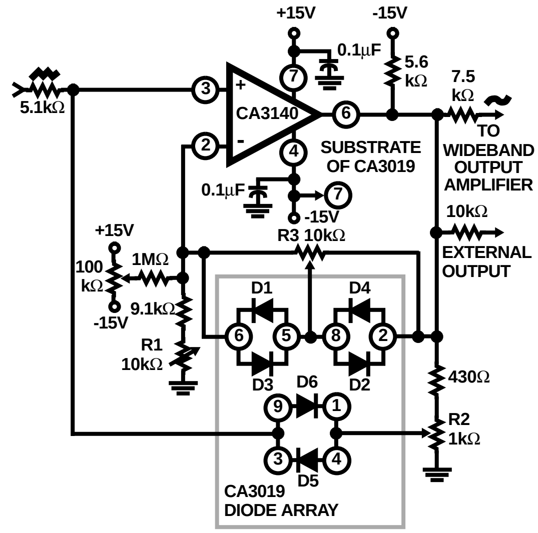



FIGURE 20. SINE WAVE SHAPER

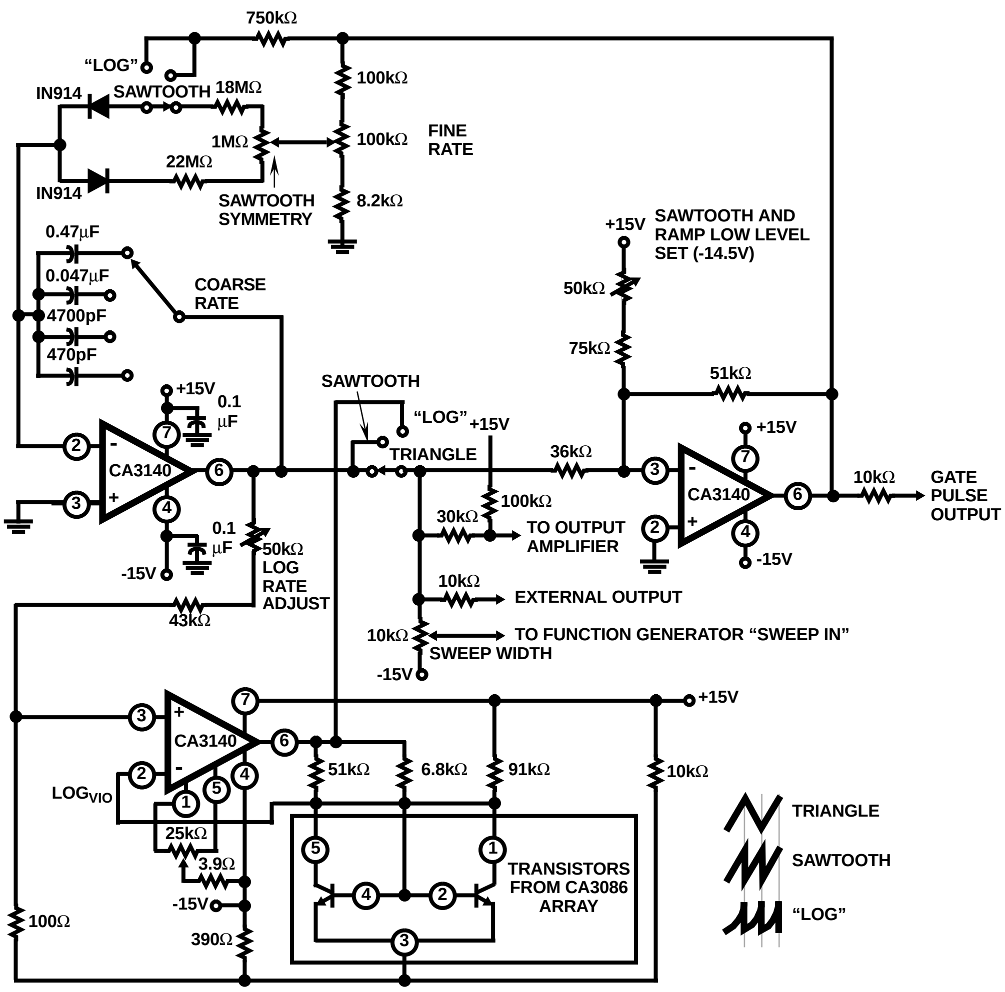



FIGURE 21. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer $R_1$, followed by an adjustment of $R_2$. The final slope is established by adjusting $R_3$, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

### Sweeping Generator

Figure 21 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

### Wideband Output Amplifier

Figure 22 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 18 and 20 provides 18V peak-to-peak output open circuited, or 9V peak-to-peak output when terminated in 50Ω. The slew rate required of this amplifier is 28V/µs (18V peak-to-peak x π x 0.5MHz).

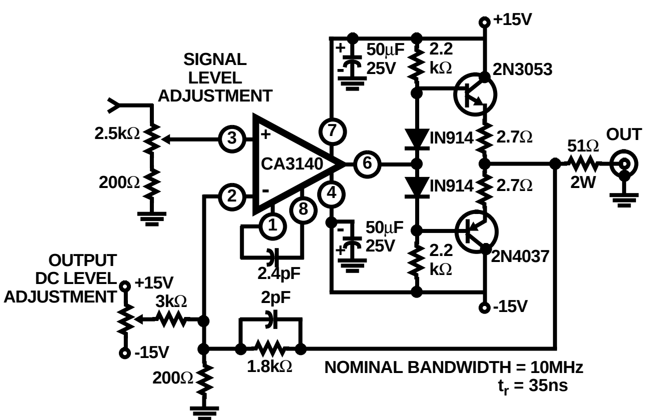



FIGURE 22. WIDEBAND OUTPUT AMPLIFIER

### Power Supplies

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in connection with the CA3140 (see Figure 23).

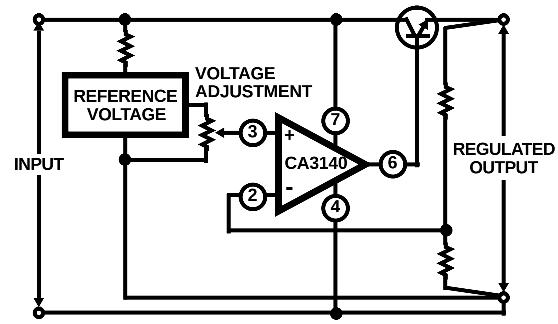



FIGURE 23. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION

Essentially, the regulators, shown in Figures 24 and 25, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high $I_{CBO}$ levels will also prevent the output voltage from reaching zero because there is a finite voltage drop ($V_{CE}$sat) across the output of the CA3140 (see Figure 10). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply rail.

Figures 24 and 25, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series pass element for the conventional current limiting system, Figure 24, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 25, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling. Fold-

back is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

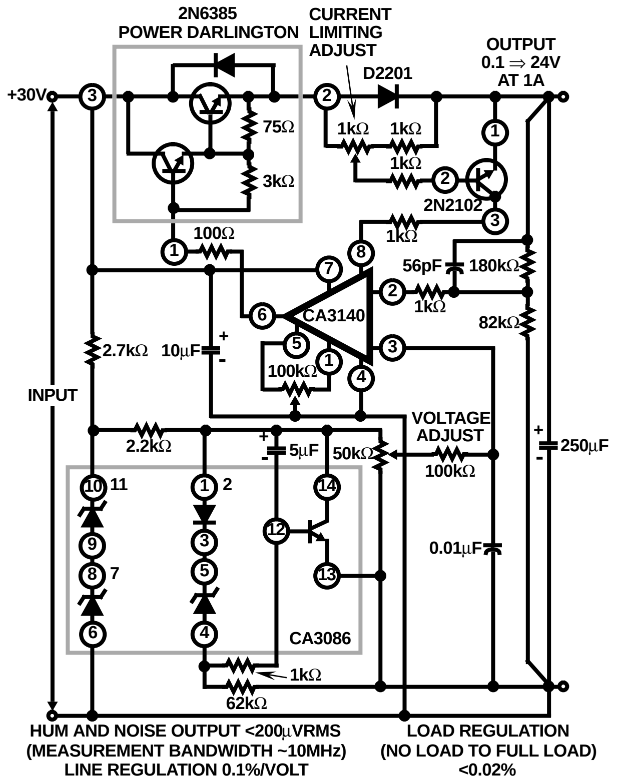



**FIGURE 24. REGULATED POWER SUPPLY**

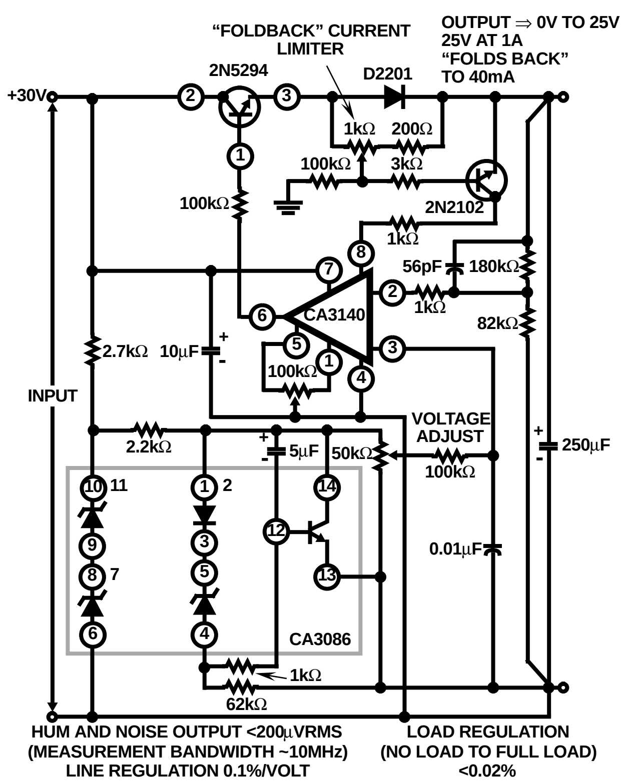
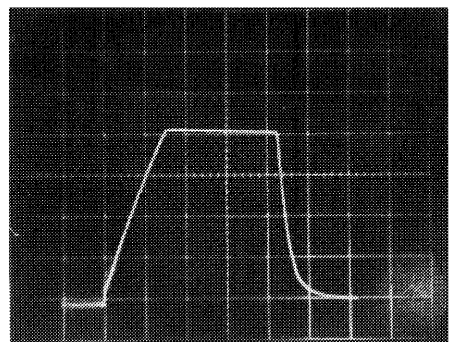



**FIGURE 25. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING**

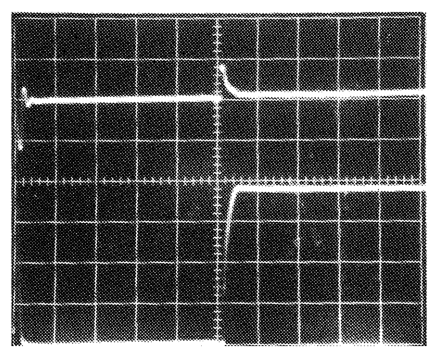
Both regulators, Figures 24 and 25, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200μV as read with a meter having a 10MHz bandwidth.

Figure 28 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 26 (B) shows the transient response of the regulator with the switching of a 20Ω load at 20V output.



**(A) SUPPLY TURN-ON AND TURNOFF CHARACTERISTICS**

5V/Div and -1s/Div



**(B) TRANSIENT RESPONSE**

Top Trace: Output voltage
200mV/Div and 5μs/Div

Bottom Trace: Collector of load switching transistor, load = 1A
5V/Div and 5μs/Div

**FIGURE 26. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 24 AND 25**

## Tone Control Circuits

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figures 27 and 28.

The first circuit, shown in Figure 28, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the CA3140. The amplifier gain is 3dB down from its "flat" position at 70kHz.

Figure 27 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No. 3 to ground. A detailed analysis of this circuit is given in "An IC Operational TransconductanceAmplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.

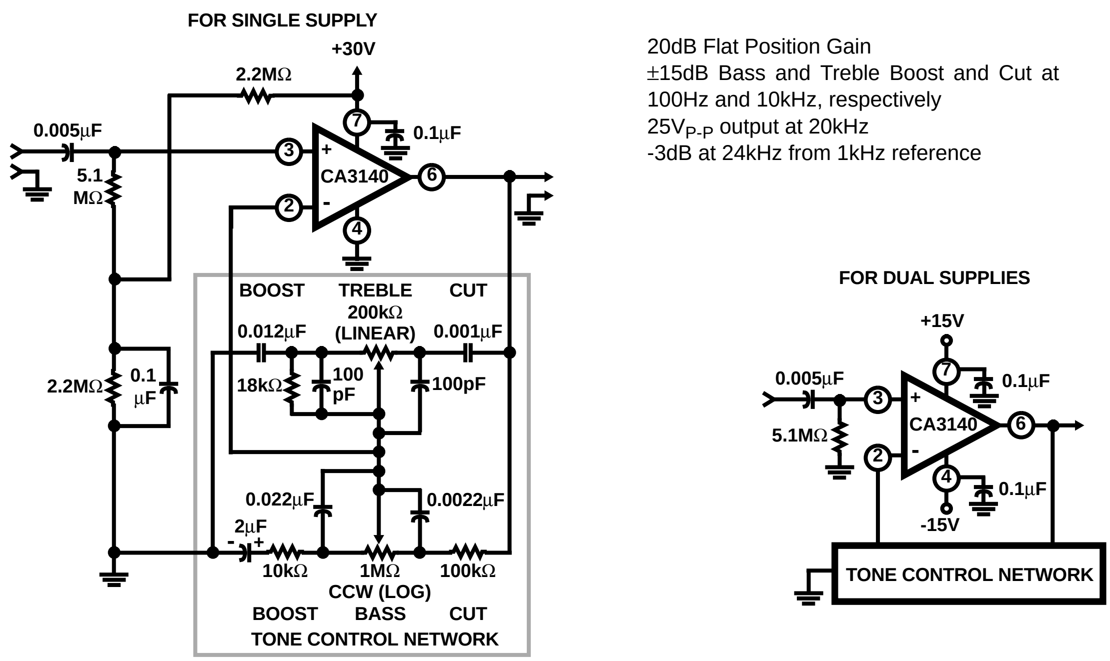



**FIGURE 27. TONE CONTROL CIRCUIT USING CA3130 SERIES (20dB MIDBAND GAIN)**

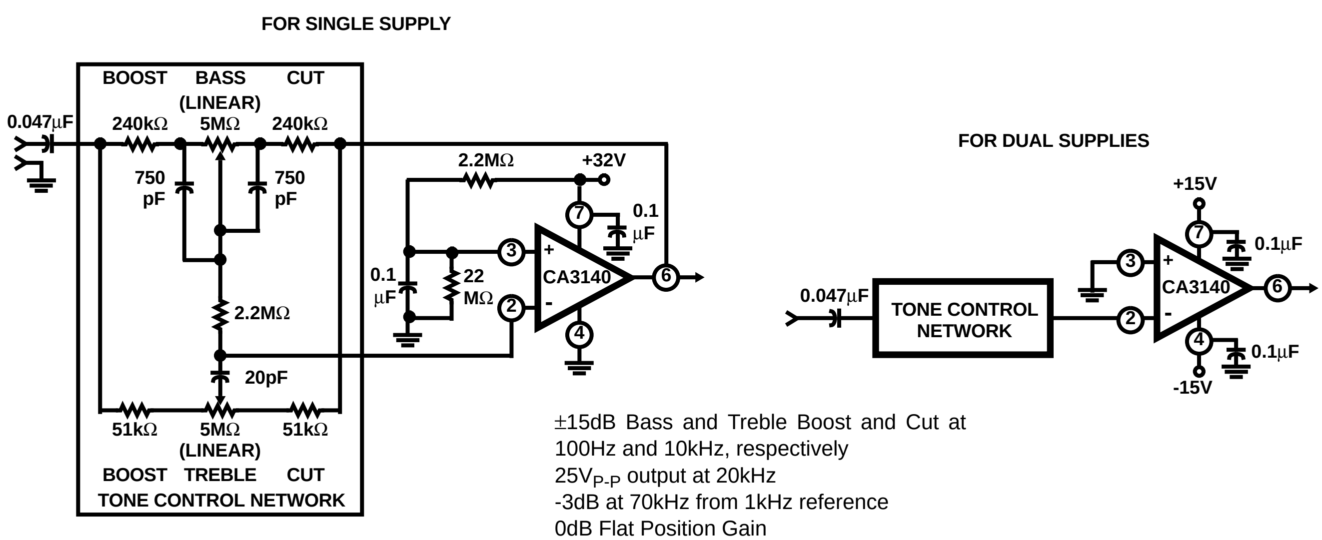
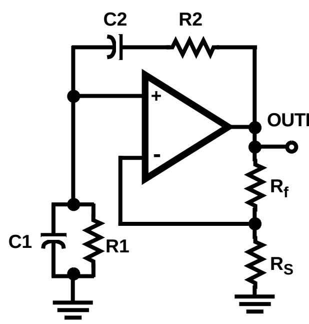



**FIGURE 28. BAXANDALL TONE CONTROL CIRCUIT USING CA3140 SERIES**

### Wien Bridge Oscillator

Another application of the CA3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 29. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, $A_{OSC}$ is equal to 3. Note that if $C_2$ is increased by a factor of four and $R_2$ is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the CA3140.




NOTES:

$$f = \frac{1}{2\pi\sqrt{R1C1R2C2}}$$

$$A_{OS} = 1 + \frac{C1}{C2} + \frac{R2}{R1}$$

$$A_{CL} = 1 + \frac{R_f}{R_S}$$

FIGURE 29. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, $R_S$, is commonly replaced with some variable resistance element. Thus, through some control means, the value of $R_S$ is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

Figure 30 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor ($R_f$ of Figure 29). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1µF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180kHz will reach a slew rate of approximately 9V/µs when its amplitude is 16V peak-to-peak.

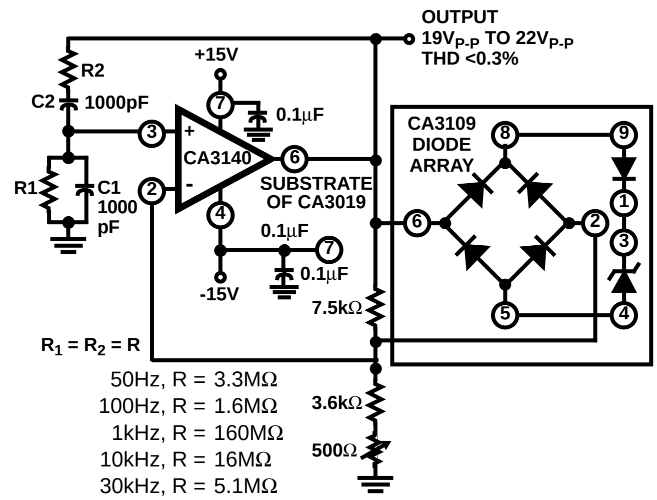



FIGURE 30. WIEN BRIDGE OSCILLATOR CIRCUIT USING CA3140 SERIES

### Simple Sample-and-Hold System

Figure 31 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2kΩ and 30pF is shown in the schematic.

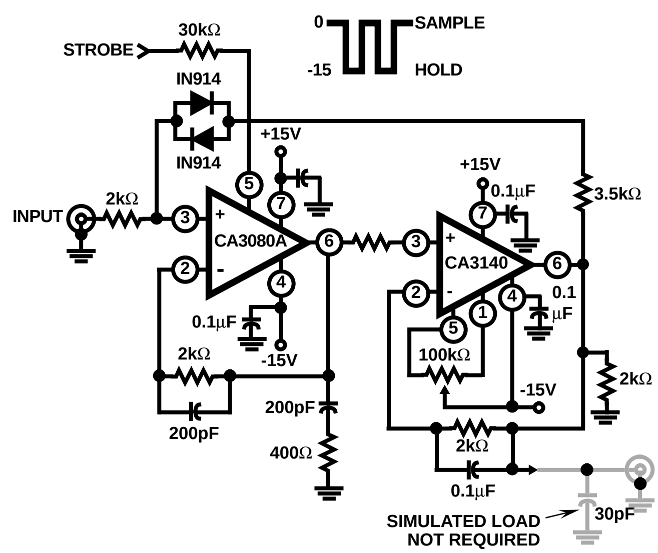



FIGURE 31. SAMPLE AND HOLD CIRCUIT

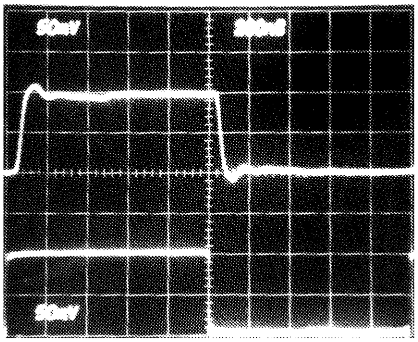
In this circuit, the storage compensation capacitance ($C_1$) is only 200pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate

$$\frac{dv}{dt} = \frac{i}{c} = 0.5mA/200pF = 2.5V/\mu s$$

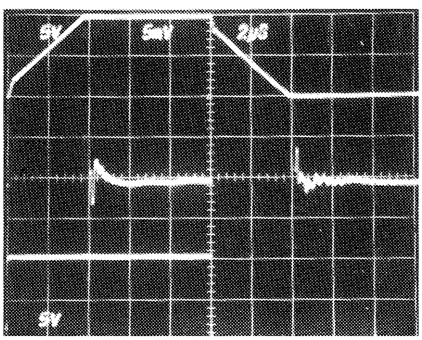
* ICAN-6668 "Applications of the CA3080 and CA 3080A High Performance Operational Transconductance Amplifiers".

Pulse "droop" during the hold interval is 170pA/200pF which is = 0.85µV/µs; (i.e., 170pA/200pF). In this case, 170pA

represents the typical leakage current of the CA3080A when strobed off. If $C_1$ were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085µV/µs, but the slew rate would decrease to 0.25V/µs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input signal feedthrough across the input terminals of the CA3080A to the 200pF storage capacitor when the CA3080A is strobed off. Figure 32 shows dynamic characteristic waveforms of this sample-and-hold system.

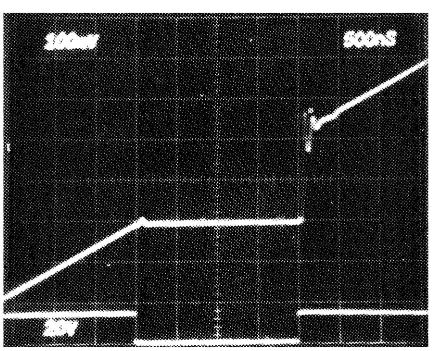


Top Trace: Output; 50mV/Div and 200ns/Div
Bottom Trace: Input; 50mV/Div and 200ns/Div



**LARGE SIGNAL RESPONSE AND SETTLING TIME**

Top Trace: Output Signal; 5V/Div and 2µs/Div
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div and 2µs/Div
Bottom Trace: Input Signal; 5V/Div and 2µs/Div



**SAMPLING RESPONSE**

Top Trace: Output; 100mV/Div and 500ns/Div
Bottom Trace: Input; 20V/Div and 500ns/Div

**FIGURE 32. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS**

### Current Amplifier

The low input terminal current needed to drive the CA3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 33.* In this circuit, low current is supplied at the input potential as the power supply to load resistor $R_L$. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100µA; a much easier current to measure in many systems.

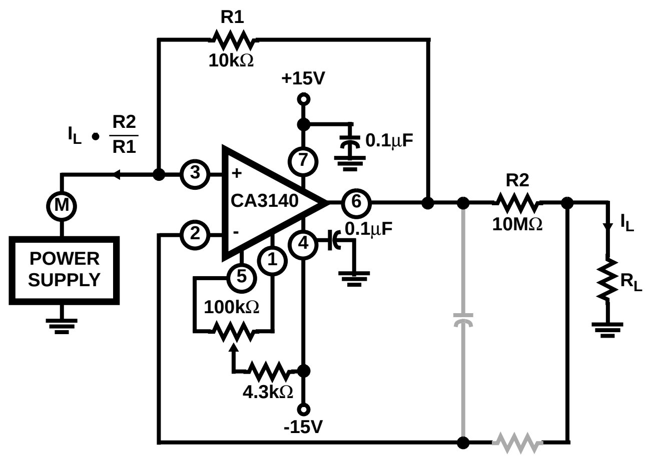


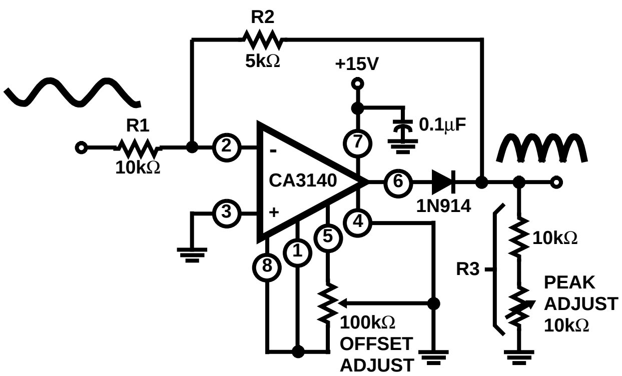

**FIGURE 33. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS**

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

Figure 34 shows a single supply, absolute value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Figure 34 is satisfied, the full wave output is symmetrical.

* "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 - "Negative Immittance Converter Circuits".




$$\text{GAIN} = \frac{R2}{R1} = X = \frac{R3}{R1 + R2 + R3}$$

$$R3 = \left(\frac{X + X^2}{1 - X}\right) R1$$

$$\text{FOR}X = 0.5 \frac{5k\Omega}{10k\Omega} = \frac{R2}{R1}$$

$$R3 = 10k\Omega\left(\frac{0.75}{0.5}\right) = 15k\Omega$$

20Vp-p Input BW(-3dB) = 290kHz, DCOutput (Avg) = 3.2V

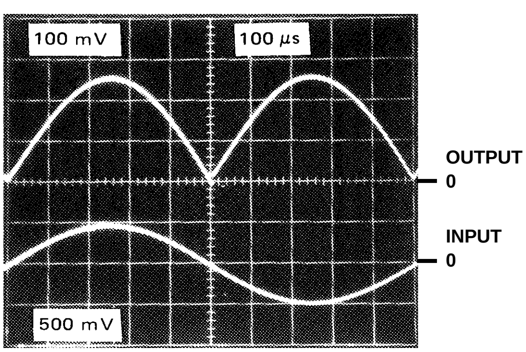



**FIGURE 34. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS**

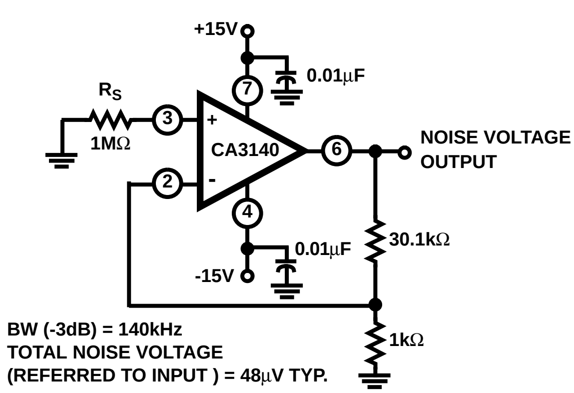
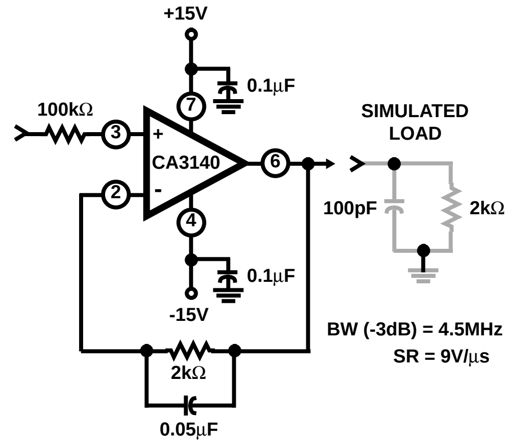
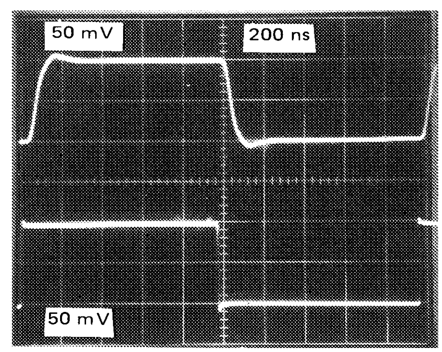


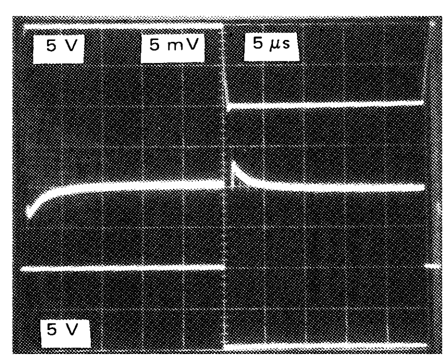

**FIGURE 35. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT**




**(A) SMALL SIGNAL RESPONSE**
50mV/Div and 200ns/Div

Top Trace: Output; 50mV/Div and 200ns/Div
Bottom Trace: Input; 50mV/Div and 200ns/Div




**(B) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME**
(measurement made with Tektronix 7A13 differential amplifier)

Top Trace: Output Signal; 5V/Div and 5µs/Div
Center Trace: Difference Signal; 5mV/Div and 5µs/Div
Bottom Trace: Input Signal; 5V/Div and 5µs/Div

**FIGURE 36. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS**